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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/022,659
Filing Date: December 18, 2001
Appellant(s): AZADET ET AL.

Kevin M. Mason
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 08/13/2007 appealing from the Office action mailed 03/02/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

Claims 1, 8, 16, 26, and 29 ate being appealed.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,418,172	RAGHAVAN	7-2002
6,377,640	TRANS	4-2002

Haratsch, "A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468.

Haratsch, "High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium on VLSI Technology, Systems, and Applications, 1999.8-10 June 1999 Page(s): 171 – 174.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 16-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan (US 6418172 B1) in view of Trans (US 6377640 B2).

As per claim 16, Raghavan discloses a method for representing an MLT-3 code as a trellis, the MLT-3 code uses three signal levels to represent two binary values (figure 1A column 3 lines 37-50), the method comprising generating the trellis with a plurality of trellis states, each of the trellis states associated with a value for a signal in a

previous symbol period (figure 1A column 3 lines 37-50); generating each of the trellis states with at least two branches leaving or entering each state, each of the at least two branches corresponding to state transitions associated with the two binary values and for each state a first binary value substantially always maintain causes a state transition in the trellis from a first state to a different state and a secondary binary value does not cause a state transition in the trellis (figure 1A column 3 lines 37-50); and using the trellis to decode a signal encoded using the MLT-3 code (figure 1A block 96 column 4 lines 22-26). Raghavan doesn't specifically disclose that always a first binary value causes a state transition and a secondary binary value does not cause a state transition. Trans discloses that always a first binary value causes a state transition and a secondary binary value does not cause a state transition (column 61 lines 48-56). Raghavan and Trans teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the transitions disclosed by Trans. The suggestion/motivation for doing so would have been to reduce the complexity and bandwidth of the system (column 61 lines 48-56).

As per claim 17, Raghavan and Trans disclose claim 16. Raghavan also discloses that a first one of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of +1 (figure 1A column 3 lines 37-50).

As per claim 18, Raghavan and Trans disclose claim 16. Raghavan also discloses that a second and third of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of 0 (figure 1A column 3 lines 37-50).

As per claim 19, Raghavan and Trans disclose claim 16. Raghavan also discloses that a fourth one of the plurality of trellis states corresponds to a value for a signal in a previous symbol period of -1 (figure 1A column 3 lines 37-50).

As per claim 22 Raghavan and Trans disclose claim 16. Raghavan also discloses an Ethernet channel (column 1 lines 11-34).

Claims 1, 7, 8, 12, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan (US 6418172 B1) in view of Haratsch ("A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468) (hereafter Haratsch1).

As per claims 1 and 8, Raghavan discloses the MLT-3 encoding (column 1 lines 24-36), Raghavan doesn't disclose decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis. Haratsch1 discloses decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis (title, abstract, introduction, parallel decision-feedback decoding

and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

As per claim 7 and 15, Raghavan and Haratsch1 disclose claims 1 and 8, Raghavan also discloses an Ethernet channel (column 1 lines 11-36).

As per claim 12, Raghavan and Haratsch1 disclose claim 1, Haratsch1 also a branch metric units (BMU) that calculates branch metrics based on said received signal (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4); an add-compare-select unit (ACSU) that determines the best surviving paths into said trellis states (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4); and a survivor memory unit (SMU) that stores said best surviving paths (figures 2 and 4 parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the joint equalization and decoding disclosed by Haratsch1. The

suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Trans as applied to claim 16 above, and further in view of Haratsch ("A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet", Proceedings of the IEEE 2000 Custom Integrated Circuits Conference, 2000. CICC, 21-24 May 2000 Page(s): 465 – 468) (hereafter Haratsch1). Raghavan and Trans disclose claim 16. Raghavan also discloses encoding a signal using MLT-3 code (figure 1A column 3 lines 37-50). Raghavan doesn't disclose using the trellis to perform joint equalization and decoding of an encoded signal. Haratsch1 discloses decoding a encoded signal received from a dispersive channel causing intersymbol interference, comprising generating at least one trellis representing the code and the dispersive channel and performing joint equalization and decoding of the received signal using the trellis (title, abstract, introduction, parallel decision-feedback decoding and joint equalizer and decoder architecture sections pages 21-2-1 to 21-2-4). Raghavan, Trans and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Trans the joint equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

Claims 2, 9, 10 and 23-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Haratsch1 as applied to claims 1 and 8 above, and further in view of Haratsch ("High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium on VLSI Technology, Systems, and Applications, 1999. 8-10 June 1999 Page(s): 171 – 174) (hereafter Haratsch2).

As per claims 2 and 9, Raghavan and Haratsch1 disclose claims 1 and 8, Raghavan and Haratsch1 don't disclose a reduced complexity sequence estimation technique. Haratsch2 discloses a reduced complexity sequence estimation technique (title, abstract, introduction, and reduced complexity sequence estimation sections pages 171-174). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claim 10, Raghavan, Haratsch1 and Haratsch2 disclose claim 9, Haratsch2 also discloses a branch metric units (BMU) that calculates branch metrics based on said received signal (reduced complexity sequence estimation section B page 172 figure 4); an add-compare-select unit (ACSU) that determines the best surviving paths into said reduced states (reduced complexity sequence estimation section B page

172 figure 4); a survivor memory unit (SMU) that stores said best surviving paths (reduced complexity sequence estimation section B page 172 figure 4); and a decision-feedback unit (DFU) that takes survivor symbols from said SMU to calculate ISI estimates for said reduced states, wherein said ISI estimates are used by said BMU to calculate branch metrics for transitions in the reduced-state trellis(reduced complexity sequence estimation section B page 172 figure 4). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 23 and 27, Raghavan and Haratsch1 disclose claims 1 and 8. Raghavan and Haratsch1 don't disclose that a state in the trellis is given by a concatenation of the code state and a channel state, where the channel state describes the dispersive channel. Haratsch2 discloses that a state in the trellis is given by a concatenation of the code state and a channel state, where the channel state describes the dispersive channel (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and

Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 24 and 28, Raghavan and Haratsch1 disclose claims 1 and 8. Raghavan and Haratsch1 don't disclose that a state in the trellis is given by a concatenation of the code state and a truncated channel state, where the truncated channel state describes the dispersive channel. Haratsch2 discloses that a state in the trellis is given by a concatenation of the code state and a truncated channel state, where the truncated channel state describes the dispersive channel (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claims 26 and 29, Raghavan, Haratsch1 and Haratsch2 disclose claims 24 and 28. Haratsch2 also discloses that that number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory (introduction section page 171). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to

incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

As per claim 25, Raghavan, Haratsch1 and Haratsch2 disclose claim 24. Haratsch2 also discloses computing ISI estimates for the states using symbols from corresponding survivor paths (introduction, and reduced complexity sequence estimation sections pages 171-172); computing branch metrics for transitions in the trellis based on the ISI estimates (introduction, and reduced complexity sequence estimation sections pages 171-172); determining survivor paths into the states based on the branch metrics; and storing the survivor paths (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Haratsch1 and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan and Haratsch1 the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Raghavan and Trans as applied to claim 16 above, and further in view of Haratsch ("High-speed VLSI implementation of reduced complexity sequence estimation algorithms with application to Gigabit Ethernet 1000Base-T", International Symposium

on VLSI Technology, Systems, and Applications, 1999. 8-10 June 1999 Page(s): 171 – 174) (hereafter Haratsch2). Raghavan discloses claim 16. Raghavan doesn't disclose combining the trellis with a trellis representing a channel to obtain a super trellis. Haratsch2 also discloses combining the trellis with a trellis representing a channel to obtain a super trellis (introduction, and reduced complexity sequence estimation sections pages 171-172). Raghavan, Trans and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the MLT-3 encoding disclosed by Raghavan and Trans the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

(10) Response to Argument

Regarding claim 16:

Applicant's arguments filed on 08/13/2007 have been fully considered but they are not persuasive.

The Applicant contends, "Appellants respectfully submit that the Examiner has failed to establish a pima facie case of obviousness for at least the reason that there exists no motivation to combine the references, and further, even if combinable, the references collectively do not teach each and every limitation of the independent claims. See, e.g., M.P.F.P. §2143. The Examiner acknowledges that Raghavan does not disclose that a first binary value substantially always causes a state transition in said

trellis from a first state to a different state and a second binary value does not cause a state transition in said trellis as required by claim 16. The Examiner asserts, however, that this feature is shown by Trans. As previously asserted by Appellants, however, (but not addressed by the Examiner at all in the Response to Arguments section of the latest Office Action), Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a trellis) Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a trellis). See, Col. 61, lines 48-56. Trans does not disclose representing an MLT-3 code using a trellis, and thus, states of state transitions axe not defined in Trans, as those terms are used by the present invention. As asserted in Appellants' prior responses, Raghavan discloses that a binary logic one (1) is transmitted as either a -1 or +1, and a binary logic zero (0) is transmitted as a 0 (see, col. 1, lines 24-36 and FIG 1A) Thus, in Raghavan (for example, Fig 1A), the input value 1 sometimes causes a transition into the same state, and sometimes a transition into a different state thus, one value does not always lead to a state transition as defined in claim 16. Raghavan thus teaches away from using Trans to achieve what is claimed by the present invention, as Raghavan does not define state transitions in the manner required by claim 16. Compare, the trellis of Raghavan to the MLT- trellis of the present invention. This "teaching away" is contrary to the combination suggested by the Examiner, even if both references are in the same field of' endeavor (Ethernet communications). Further, even if combinable, the references collectively do not teach each and every limitation of the

independent claims As indicated above, Trans does not disclose representing an MLT-3 code using a trellis, and thus, states or state transitions are not defined in trans, as those terms are used by the present invention. Rather, Trans teaches that each time a logic "1" is encoded, a transition (equal to an output value transition) will take place (there is no mention of causing a state transition in a trellis) Likewise, each time a logic 0 is encoded, the previous output level will be maintained for another bit period (again, there is no mention of causing a state transition in a trellis). See, Col., 61, lines 48-56 thus, Raghavan and Trans, alone or in combination, do not disclose or suggest "generating each of said trellis states with at least two branches leaving or entering each state, each of said at least two branches corresponding to state transitions associated with said two binary values, wherein a first binary value substantially always causes a state transition in said trellis from a first state to a different state and a second binary value does not cause a state transition in said trellis," as required by claim 16"

The Examiner disagrees and asserts, that, as indicated in the previous Office action, Raghavan and Trans teachings are analogous art because they are from the same field of endeavor of Ethernet communications. Ethernet communications is a very specific and very narrow field. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the transitions disclosed by Trans. The suggestion/motivation for doing so would have been to reduce the bandwidth and the complexity of the system (column 61 lines 48-56).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Raghavan also discloses that for each particular state, a first binary value substantially always maintain causes a state transition in the trellis from a first state to a different state and a secondary binary value does not cause a state transition in the trellis.

That is the reason it always a diagonal line leaving each state (a first binary value substantially always causes a state transition in the trellis from a first state to a different state), and an horizontal line leaving each state (a secondary binary value does not cause a state transition in the trellis) and diagonal line leaving each state.

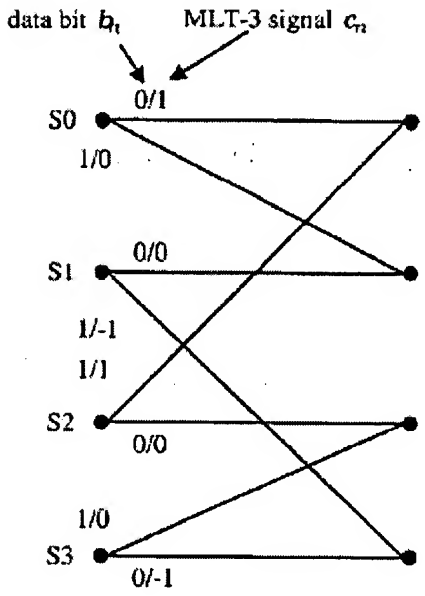
The specification doesn't provide disclosure that for all the states a first binary value substantially always causes a state transition in the trellis from a first state to a different state, and that for all the states a secondary binary value does not cause a state transition in the trellis.

Given a carefully consideration to the drawings, the Examiner uses Tran to proof that in the same very specific art, one person with ordinary skills will know that a first binary value substantially always causes a state transition and that for all the states a secondary binary value does not cause a state transition.

It is something well now in this art and a person of ordinary skill in the art will use this "state machine" that one binary value will cause a transition and the other will not. So it is common sense to use this combination because will reduce the complexity of the state machine of the trellis, because for all the states is always the same rule.

The trellis structure in the drawings is and the trellis structures of the reference used is:

Drawings of present application



Raghavan Reference

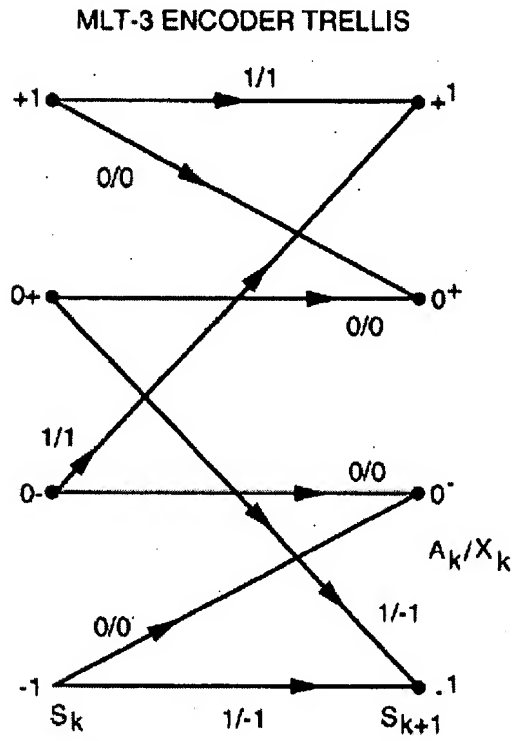


FIG. 1A (PRIOR ART)

It can be seen that the structure is identical and for the same type of coding. The reference also indicates that this structure is "prior art", so the trellis representation of the MLT-3 is well known in the art. The only difference if we give a carefully consideration to the drawing (this is not disclosed in the specification) is the state machine, that is a clear implementer choice and was also known in the same specific art, that always one the same binary value will cause a transition and the other will not. The Examiner uses Trans to disclose that feature. That doesn't produce a substantial

change in the system and it is not important in the Applicant disclosure, because it is never discloses that that change in the state machine is important.

It is well known that MLT-3 codes can be represented with a trellis structure in the same way that TCM codes, so it make prefect sense to interchange the TCM code with the MLT-3 code, because both admit a trellis representation. So the combination is absolutely proper and is a strong common sense to use either code, because both coding techniques are well know to one of ordinary skill in the art (see also KSR Int'l Co. v. Teleflex Inc. Case cited as 550 US (2007)).

For these reasons and the reason stated en the previous Office action, the rejection of claim 16 is maintained.

Regarding claims 1 and 8:

Applicant's arguments filed on 08/13/2007 have been fully considered but they are not persuasive.

The Applicant contends, "Appellants respectfully submit that the Examiner has failed to establish a prima facie case of obviousness, for at least the reason that there exists no motivation to combine the references. See, e.g. M.P E,P, §2143, First, as asserted in Appellants' prior responses, MLT-3 codes axe not trellis coded modulation (TCM) as described by Haratsch 1. Thus, it would not be obvious to a person of ordinary skill in the art to generate a trellis representing the MLT-3 and dispersive channel, in the manner suggested by the present invention. Furthermore, Haratsch 1 is addressing four dimensional TCM codes with 8 states. Thus, the corresponding computations disclosed by Haratsch 1, such as the blanch metric computations, do not

make sense in the context of the present invention, for example, Equations 1 and 2 of Haratsch 1 do not make sense for MLT-3 codes, as they show the computation of the 1D ISI estimates and 1D branch metrics for each of the 4 dimensions. Page 466, left column, then shows how to combine the 1D branch metric to obtain 4D branch metrics for the 4D TCM code, which again does not make sense for MLT-3 codes See also figures 2 and 4, where one and four dimensional branch metric units ate shown. In addition, as discussed hereinafter if the combination was attempted in the manner suggested by the Examiner, an expression is obtained for the number of states that does not make sense, The number of trellis states in Haratsch 1 is equal to the number of TCM code states and therefore equal to 8 In the present invention, on the other hand, the number of trellis states is $4x(2^K)$, where K is the truncated channel memory these incompatibilities between the combination of Raghavan/Haratsch 1 is contrary to the combination suggested by the Examiner, even if both cited references are in the same field of endeavor' (Ethernet communications). Thus, a person of ordinary skill in the art would not make such a combination In addition to providing a different number of states, which suggests away from the combination, the minimum number of states associated with the present invention ($4\times(2^K)=4$ for K=0) is lower than Haratsch 1, This is a "surprising result" which is further evidence of non-obviousness, This was not addressed by the Examiner in the Response to Arguments section of the latest Office Action, Furthermore, the Examiner asserts that the motivation for combining Raghavan with Haratsch 1 would be to reduce the complexity of the system, Rather, claims 1 and 8 in fact generally increase the complexity of the system (joint equalization and

decoding using a trellis representing both the MLT-3 code and dispersive channel) compared to a prior alt system with a MLT-3 decoder and separate equalizer".

The Examiner disagrees and asserts, that:

claim 1 claims "A method for decoding a signal received from a dispersive channel causing intersymbol interference, said signal encoded using an MLT-3 code, said method comprising the steps of: generating at least one trellis representing both said MLT-3 code and said dispersive channel; and performing joint equalization and decoding of said received signal using said trellis";

and claim 8 claims "A receiver for' processing a signal received from a dispersive channel, said signal encoded using an MLT-3 code, comprising: a sequence detector that performs joint equalization and decoding of said received signal using at least one trellis representing both said MLT-3 code and said dispersive channel"

In these very broad claims, claim 1 and claim 8 the only thing claiming is the use of the MLT-3 code with joint equalization and decoding. Two features that are very well known in the very specific field of Ethernet communications, as presented by the Examiner in the referenced used.

The secondary reference used by the examiner teaches the used of joint equalization and decoding to reduce the complexity of the system, that is well known and is a very strong motivation, that makes sense in the well known MLT-3 system.

As indicated previously, it is well known that MLT-3 codes can be represented with a trellis structure in the same way that TCM codes, so it make prefect sense to interchange the TCM code with the MLT-3 code, because both admit a trellis

representation. So the combination is absolutely proper and is a strong common sense to use either code, because both coding techniques are well know to one of ordinary skill in the art (see also KSR Int'l Co. v. Teleflex Inc. Case cited as 550 US (2007)).

About the details of the combination argued by the applicant they are not claimed in claim 1 and 8. As indicated previously claims 1 and 8 exclusively claims the combination of MLT-3 and joint equalization and decoding. As proof by the Examiner the combination is perfectly proper, because both codes, MLT-3 and TCM admit a trellis representation, so to interchange one for the other is just obvious and it is common sense.

The reason to combine used by the Examiner is that the use of joint equalization and decoding reduce the complexity of the system as indicated event in the title by the secondary reference "A low complexity joint equalizer and decoder for 1000Base-T Gigabit Ethernet" that "one-tap parallel decision-feedback decoder jointly decodes the Trellis and cancels the ISI due to the first tap of the post-cursor channel impulse response". Taking into account that TCM and MLT-3 both admit a trellis representation the combination make perfect sense.

As indicated in the previous Office action, Raghavan and Haratsch1 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. As indicated previously Ethernet communications is a very specific field At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the joint

equalization and decoding disclosed by Haratsch1. The suggestion/motivation for doing so would have been to reduce the complexity of the system (Haratsch1 abstract).

it is well known that MLT-3 codes can be represented with a trellis structure in the same way that TCM codes, so it make prefect sense to interchange the TCM code with the MLT-3 code, because both admit a trellis representation. So the combination is absolutely proper and is a strong common sense to use either code, because both coding techniques are well know to one of ordinary skill in the art.

Haratsch1 discloses joint equalization and decoding using TCM codes and, as indicated previously, it is well known that MLT-3 codes can be represented with a trellis structure in the same way that TCM codes, so it make prefect sense to interchange the TCM code with the MLT-3 code, because both admit a trellis representation. So the combination is absolutely proper and is a strong common sense to use either code, because both coding techniques are well know to one of ordinary skill in the art (see also KSR Int'l Co. v. Teleflex Inc. Case cited as 550 US (2007)).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "branch metric") are not recited in the rejected claim(s). Although the claims are

interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

For these reasons and the reason stated en the previous Office action, the rejection of claims 1 and 8 are maintained.

Regarding claims 26 and 29:

Claim 26 and claim 29 claims "a number of states in said trellis is given by $4X(2^K)$, where K is the truncated channel memory"

Applicant's arguments filed on 08/13/2007 have been fully considered but they are not persuasive.

The Applicant contends, "With respect to claims 26 and 29, for example, the Examiner assets that Hatatsch2 discloses that the number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory (citing page 171) In the passage of Halatsch2 recited by the Examiner, however, the number of states is given by $Sx(2^{mL})$, where S is the number of TCM code states, m the number of bits that are fed into the TCM encoder, and L is the (full) channel memory m is defined in Fig2 of Haratsch 2 for TCM codes, but is undefined fm MLT-3 codes, which me different from TCM codes., Significantly, the equation in page 171 of Haratsch 2 uses the channel memory L, while claims 26 and 29 use the truncated channel memory K. Therefore, the equation in page 171 of Haratsch 2 is different and undefined for MLT-3 codes. This was not addressed by the Examiner in the Response to Arguments section of the latest Office Action".

The Examiner disagrees and asserts, that, as indicated previously, it is well known that MLT-3 codes can be represented with a trellis structure in the same way that

TCM codes, so it make prefect sense to interchange the TCM code with the MLT-3 code, because both admit a trellis representation. So the combination is absolutely proper and is a strong common sense to use either code, because both coding techniques are well know to one of ordinary skill in the art (see also KSR Int'l Co. v. Teleflex Inc. Case cited as 550 US (2007)).

Raghavan and Haratsch2 teachings are analogous art because they are from the same field of endeavor of Ethernet communications. Ethernet communications is a very specific field. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate in the MLT-3 encoding disclosed by Raghavan the reduced complexity sequence estimation technique disclosed by Haratsch2. The suggestion/motivation for doing so would have been to reduce the hardware complexity of the algorithm (Haratsch2 abstract).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

A resented by Raghavan the number of states is 4 so in the equation provide by Haratsch2 S=4. Taking into account that the TCM and MLT-3 can be interchanged because both admit a trellis representation, Using Haratsch2 with the reduce state sequence estimation RSSE section B in page 172 the "RSSE [3][4] reduces the complexity, of the MLSE by merging multiple states of the full combined channel/code

trellis. Decision-feedback sequence estimation (DFSE) is a specialization of RSSE and employs a trellis that takes into account only the first K of the L channel coefficients $\{f_k\}$, $0 \leq K \leq L$. The combination of the code state and truncated channel state defines the reduced combined state"

So using the proper combination of the references in a truncated channel estate the number of states in the trellis is given by $4x(2^K)$, where K is the truncated channel memory.

It is noted that as indicated by the applicant ("where K is referred to as truncated channel memory. The number of states in the reduced-state trellis is $4x2^K$. When K is chosen to be 0, the reduced-state trellis simplifies to the MLT-3 code trellis of FIG. 4" see page 6 lines 15-21) and as shown by Raghavan (figure 1A) .

As indicated by Haratsch2 ("A special case arises when K = 0, where the reduced trellis becomes the TCM code trellis and decision-feedback equalization is performed for each code state based on the survivor history of that path. This is called parallel decision-feedback equalization (PDFE)" page 172 column 1 section B first paragraph) if K=0 the number of states are 4. Again TCM and MLT-3 are interchanged because both, as will be recognized by one of ordinary skill in the art admit trellis representation.

For these reasons and the reason stated en the previous Office action, the rejection of claims 26 and 29 are maintained.

Regarding Dependent claims:

Applicant's arguments filed on 08/13/2007 have been fully considered but they are not persuasive.

The Applicant contends, "Claims 2, 7, 9-10, 12, 15 and 17-29 me dependent on claims 1, 8, or 16, and are therefore patentably distinguished over Raghavan, Haratsch 1, Trans, and Haratsch 2 (alone or in any combination) because of their dependency from independent claims 1, 8, and 16 for the reasons set forth above, as well as other elements these claims add in combination to their base claim".

The Examiner disagrees and asserts, that, as indicated previously, because the rejections of claims 1, 8 and 16 are maintained, the rejection of claims 2, 7, 9-10, 12, 15 and 17-29 are also maintained.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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08-14-2007

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